DATA SHEET

TDA8042M
Quadrature demodulator

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

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Quadrature demodulator TDA8042M

FEATURES

- 5 V supply voltage
- Internal voltage reference
- 350 to 650 MHz input frequency range
- On-chip 0° and 90° phase shifter
- Symbol rate up to 45 Msymbols/s
- High input sensitivity
- Built-in voltage stabilizer
- AGC amplifier with 21 dB control range
- AGC detector.

APPLICATION

- Binary Phase-Shift Keying (BPSK) and Quadrature Phase-Shift Keying (QPSK) demodulation.

GENERAL DESCRIPTION

The TDA8042M is a monolitic bipolar IC dedicated for BPSK and QPSK demodulation. It is designed to be used together with the TDA8043 as part of a complete BPSK/QPSK satellite demodulator and decoder.
The bandwidth of the TDA8042M allows symbol rates up to 45 Msymbols/s. It includes two matched mixers, an IF gain controlled amplifier, a symmetrical oscillator, a 0°/90° phase shifter, two low-pass filters and two matched baseband amplifiers.

The high input sensitivity makes interfacing with various sources easy. The input sensitivity can be adjusted by means of an internal AGC amplifier.

The oscillator operates at half the IF frequency. The local oscillator signal driving the mixers is made by doubling the oscillator frequency by an internal frequency multiplier. The oscillator frequency can be set by the appropriate external LC tank circuit. The internal wideband phase shifter provides two oscillator signals which are 90 degrees out of phase to drive the mixers.

An AGC detector at the I and Q outputs makes it possible to keep the I and Q signals at a constant level to drive the analog-to-digital converters of the TDA8043.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.75	5.0	5.25	V
I_{CC}	supply current	V_{CC} = 5.0 V	54	67.5	81	mA
$V_{i(RF)}$	operating input level		–	57	–	dBμV
$f_{i(RF)}$	RF input signal frequency		350	–	650	MHz
$V_{oIQ(p-p)}$	I and Q output voltage (peak-to-peak value)		–	0.8	–	V
$\Delta E_{\Phi(I-Q)}$	phase matching error between I and Q channels		–	0.7	2	deg
$\Delta E_{G(I-Q)}$	gain matching error between I and Q channels		–	0.15	0.8	dB
ΔG_{tilt}	gain tilt error between I and Q channels		–	0.3	0.5	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8042M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

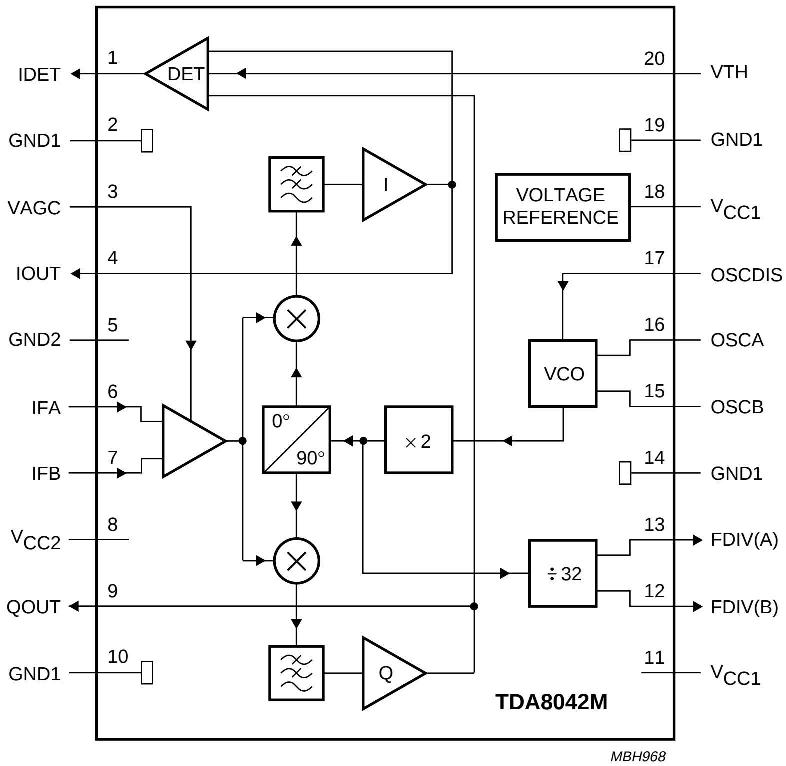


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IDET	1	AGC detector output signal
GND1	2	ground
VAGC	3	gain control input voltage
IOUT	4	I channel amplifier output
GND2	5	ground
IFA	6	IF input A
IFB	7	IF input B
V_{CC2}	8	supply voltage 2
QOUT	9	Q channel amplifier output
GND1	10	ground
V_{CC1}	11	supply voltage 1
FDIV(B)	12	prescaler output B
FDIV(A)	13	prescaler output A
GND1	14	ground
OSCB	15	oscillator tank circuit B
OSCA	16	oscillator tank circuit A
OSCDIS	17	oscillator disable input
V_{CC1}	18	supply voltage 1
GND1	19	ground
VTH	20	AGC threshold voltage input

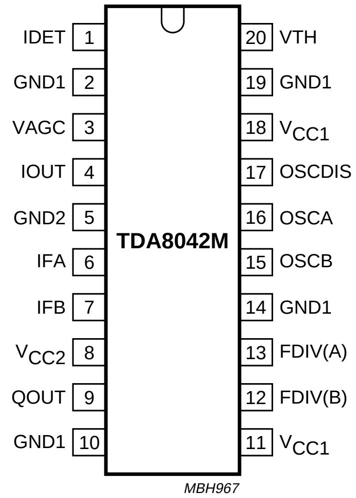


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	+6.0	V
V_i	input voltage on all pins	–0.3	V_{CC}	V
P_{tot}	total power dissipation	–	470	mW
T_{stg}	IC storage temperature	–55	+150	°C
T_j	junction temperature	–	+150	°C
T_{amb}	operating ambient temperature	0	+70(1)	°C

Note

1. The operating ambient temperature can be extended up to +85 °C providing the supply voltage remains lower or equal to 5.2 V in order to maintain the junction temperature below 150 °C.

QUALITY SPECIFICATION

All pins withstand the ESD test in accordance with *“UZW-BO/FQ-A302 (human body model)”* and with *“UZW-BO/FQ-B302 (machine model)”*. These numbers can be found in the *“Quality reference Handbook”*. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	120	K/W

CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; $R_{L(IQ)}$ = 1 kΩ; measured in application circuit of Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC1}	supply voltage		4.75	5.0	5.25	V
V_{CC2}	supply voltage		4.75	5.0	5.25	V
I_{CC1}	supply current	$V_{CC1} = V_{CC2}$ = 5.0 V	41	51	61	mA
I_{CC2}	supply current	$V_{CC1} = V_{CC2}$ = 5.0 V	13	16.5	20	mA
AGC						
G_{CR}	gain control range		21	29	–	dB
G_{VAGC}	voltage gain control at pin 3	note 1				
	input level = $V_{i(RF)min}$		0.5	–	2	V
	input level = $V_{i(RF)max}$		3.5	–	4.5	V
R_{iVAGC}	input resistance at pin 3		–	20	–	kΩ
V_{th}	AGC threshold voltage	note 2				
	V_o = 1.6 V (peak-to-peak value)		–	3.6	–	V
	V_o = 0.8 V (peak-to-peak value)		–	2.4	–	V
	V_o = 0.4 V (peak-to-peak value)		–	1.8	–	V
R_{iVTH}	VTH input resistance		–	10	–	kΩ
$\|I_{det}\|$	maximum AGC detector output current (absolute value)	note 3	–	1	–	mA
QPSK demodulator						
$f_{i(RF)}$	RF input signal frequency		350	–	650	MHz
$R_{i(RF)}$	RF input impedance (resistive part)	$f_{i(RF)}$ = 480 MHz	–	50	–	Ω
$X_{i(RF)}$	RF input impedance (reactive part)	$f_{i(RF)}$ = 480 MHz	–	19	–	Ω
$V_{i(RF)}$	operating RF input level	note 1	57	–	78	dBμV
$\Delta E_{\Phi(I-Q)}$	phase matching error between I and Q channels	note 4	–	0.7	2	deg
$\Delta E_{G(I-Q)}$	gain matching error between I and Q channels	note 5	–	0.15	0.8	dB
ΔG_{tilt}	gain tilt error between I and Q channels	note 6	–	0.3	0.5	dB
F	DSB noise figure	source impedance = 50 Ω; note 7	–	13	17	dB
$d_{3(IQ)}$	third-order intermodulation distortion in I and Q channels	note 8	–	50	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
f_{osc}	oscillator frequency	note 9	175	–	325	MHz
Δf_{osc}	frequency drift	note 10	–	–	500	kHz
		ΔV_{CC} = ±5%	–	–	100	kHz
N_{osc}	oscillator phase noise	measured10 kHz from f_{osc}; note 11	–	–	91	dBc/Hz
$V_{osc(dis)}$	oscillator disable voltage at pin 17					
	oscillator disabled		–	–	1.0	V
	oscillator enabled		4.0	–	–	V
Prescaler						
V_{OH}	HIGH level output voltage	note 12	4.0	–	–	V
V_{OL}	LOW level output voltage	note 12	–	–	3.35	V
δ	output duty cycle		40	50	60	%
$DIV_{spu(IQ)}$	output spurious voltage at I and Q outputs	note 13	–	–50	–	dB
I and Q internal filters						
B_{-1}	bandwidth for 1 dB attenuation		30	–	–	MHz
B_{-30}	bandwidth for 30 dB attenuation		–	450	–	MHz
I and Q output amplifiers						
$V_{O(IQ)(DC)}$	I and Q channels DC output voltage		–	2.45	–	V
$V_{o(IQ)(p-p)}$	I and Q channels output voltage (peak-to-peak value)	note 14	–	0.8	–	V
$V_{clip(p-p)}$	I and Q output clipping level (peak-to-peak value)		1.8			V
$R_{L(IQ)}$	I and Q channels output load resistance	note 15	500	–	–	Ω
$R_{o(IQ)}$	I and Q channels output resistance		–	67	–	Ω
$\alpha_{ct(I-Q)}$	crosstalk between I and Q channels		30	–	–	dB

Notes

1. The voltage gain control range (G_{VAGC}) is defined as the DC voltage to be applied on pin 3 to get a signal level of 800 mV (peak-to-peak value) at I and Q outputs.
   The lowest control voltage corresponds to the highest sensitivity and gain.
2. V_{th} is the level of voltage to be applied at pin 20 to get a current I_{det} of 0.5 mA at pin 1. This voltage depends on the amplitude of the signal at I and Q outputs.
   The AGC threshold voltage can be set by a resistive voltage divider connected at pin 20. Without the external resistors V_{th} is set at a value close to 2.35 V.
3. The current I_{det} increases when the output level (at pins 4 and 9) increases above the value set by the adjustment of V_{th}.
4. The phase error is defined as the phase quadrature imbalance between I and Q channels.
5. The gain error is defined as the phase quadrature imbalance between I and Q channels.
6. The tilt is defined as the difference between the maximum and the minimum channel gain measured in a frequency band of ±30 MHz around $f_{i(RF)}$. The specified tilt is the maximum tilt value found in one of the I and Q channels.

7. The specified noise figure is the maximum value obtained from I and Q channels noise measurement. The figure holds for the maximum gain (G_{VAGC} = 0.5 V).
8. The specified intermodulation distortion is the minimum value obtained from intermodulation measurements in I and Q channels. The specified value is the minimum distance between wanted signal and intermodulation products measured at the output for a wanted output level of 0.8 V (peak-to-peak value).
9. The oscillator is tuned with an appropriate tank circuit designed for each frequency limit.
10. The drift of the oscillator frequency with temperature is defined for ΔT_{amb} = 25 °C. It is measured in the application circuit (see Fig.4) with a temperature compensated tank circuit. The temperature compensation used for this measurement is realized using the application which is depicted in Fig.3.
11. The phase noise is measured at the oscillator frequency (= 240 MHz). Due to the internal frequency doubler the phase noise at the input of the mixers will be 6 dB worse.
12. Measured with a high impedance load (R_L > 5 kΩ) connected at pins 12 and 13.
13. The prescaler output spurious voltage at I and Q outputs are measured with respect to an output level of 800 mV (peak-to-peak value).
14. Measured with an input signal $f_{i(RF)}$ + 500 kHz (i.e. 480.5 MHz).
15. The load should be AC-coupled.

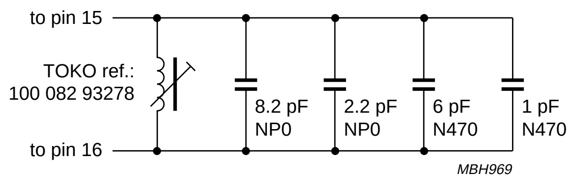


Fig.3 Temperature compensation circuit.

APPLICATION INFORMATION

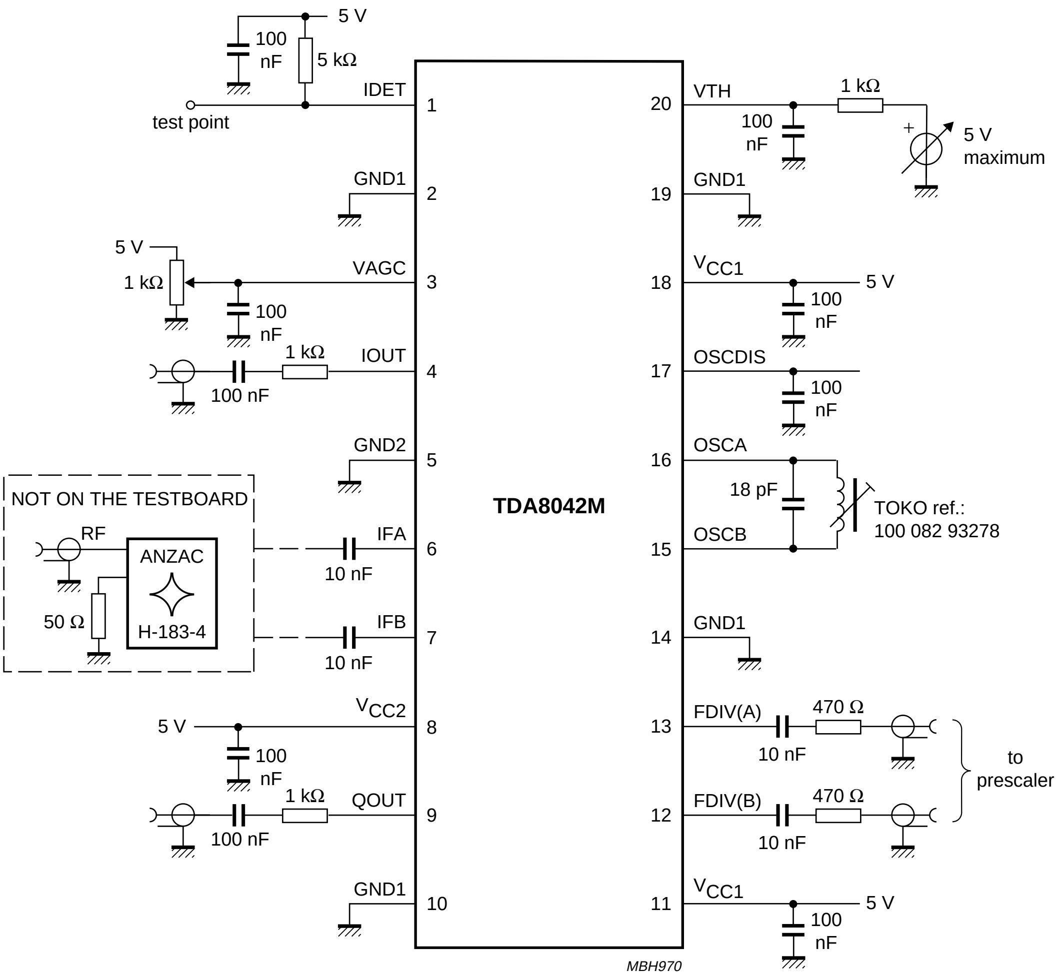
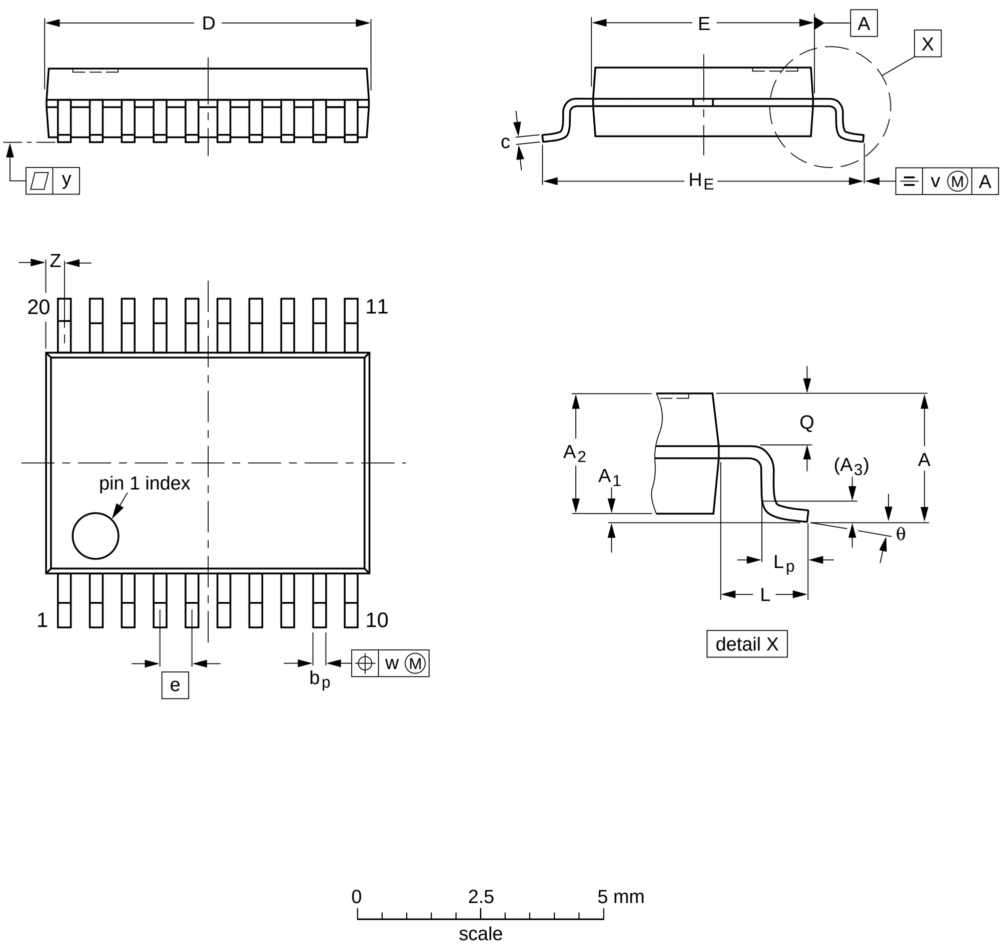


Fig.4 Application diagram.

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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