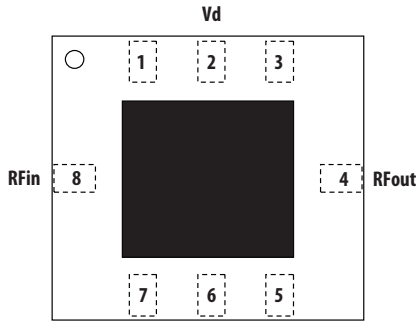
AMMP-5620
6 – 20 GHz High Gain Amplifier in SMT Package

Data Sheet

Description

The AMMP-5620 MMIC is a GaAs wide-band amplifier in a surface mount package designed for medium output power and high gain over the 6-20 GHz frequency range. The 3 cascaded stages provide high gain while the single bias supply offers ease of use. It is fabricated using a PHEMT integrated circuit process. The RF input and output ports have matching circuitry for use in 50-ohms environments. The MMIC is a cost effective alternative to hybrid (discrete FET) amplifiers that require complex tuning and assembly processes.

Package Diagram



Pin	Function
1	
2	Vd
3	
4	RF_out
5	
6	
7	
8	RF_in

RoHS-Exemption

Please refer to hazardous substances table on page 7.

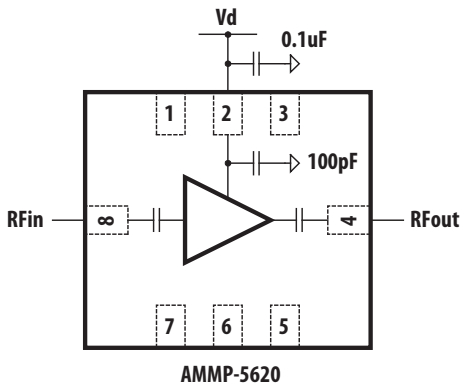
Features

- Surface Mount Package, 5.0 x 5.0 x 1.25 mm
- Wide Frequency Range 6-20 GHz
- High Gain: 17.5 dB Typical
- Medium Output P1dB: 14.8 dBm Typical
- Input and Output Return Loss: <-10 dB Typical
- 50 Ohm Input and Output Match
- Single Supply Bias: 5V @ 95 mA Typical

Applications

- General purpose, wide band amplifier in communication systems or microwave instrumentation
- High Gain Amplifier

Functional Block Diagram



Note: Package base: GND

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (40V)
ESD Human Body Model (150V)
Refer to Avago Application Note A004R: Electrostatic Discharge, Damage and Control.

Note: MSL Rating = Level 2A

Electrical Specifications

1. Typical value determined from a sample size of 500 parts from 2 wafers.
2. Small/large signal data measured in a fully de-embedded test fixture at TA = 25 degree Celsius.
3. Specifications are derived from measurements in a 50 Ohm test environment. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity, or low noise matching.
4. All tested parameters guaranteed with measurement accuracy ± 0.5 dB for NF and ± 1.0 dB for gain.

Table 1. RF Electrical Characteristics

Parameter	Min	Typ.	Max	Unit
Small-signal Gain, Ga	15.5	17.5	19.5	dB
Noise Figure, NF		5.1	7.0	dB
Output Power at 1dB Gain Compression, P-1dB		14.8		dBm
Third Order Intercept Point, OIP3		22.5		dBm
Input Return Loss, RLin		11.5		dB
Output Return Loss, RLout		11.6		dB
Reverse Isolation, Isol		-43.0		dB

Table 2. Recommended Operating Range

Description	Pin	Min.	Typical	Max.	Unit
Drain Supply Voltage, Vdd	Vd		5		V
Drain Supply Current, Idd		70	95	130	mA

Notes:
1. Ambient operation temperature TA = 25°C unless otherwise noted.
2. Channel-to-board Thermal Resistance is measured using Infrared Microscopy method.

Table 3. Thermal Properties

Parameter	Test Conditions	Value
Thermal Resistance, $\theta_{ch\text{-}b}$		$\theta_{ch\text{-}b}$ = 28 °C/W

Absolute Minimum and Maximum Ratings

Table 4. Minimum and Maximum Ratings

Description	Pin	Min.	Max.	Unit	Comments
Drain Supply Voltage	Vd		7.5	V	
Total Drain Current, Idd			135	mA	
RF Input Power (Pin)	RF_{IN}		20	dBm	CW
Power Dissipation (Pdc)		1.0	W		
Channel Temperature		+150	°C		
Storage Temperature	-65	+150	°C		
Maximum Assembly Temperature		+260	°C		

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device. The absolute maximum ratings for Vdd, Idd, Pdc and Pin were determined at an ambient temperature of 25°C unless noted otherwise.

Selected performance plots

All data measured on at Vdd = 5V, Idd = 95mA, Ta = 25oC, and 50 Ω at all ports.

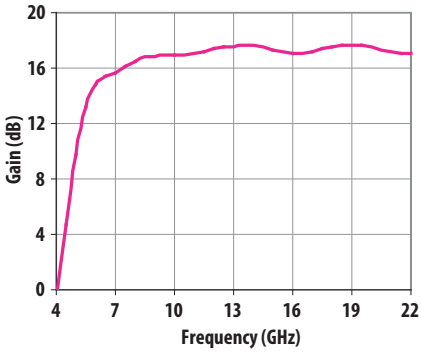


Figure 1. Gain

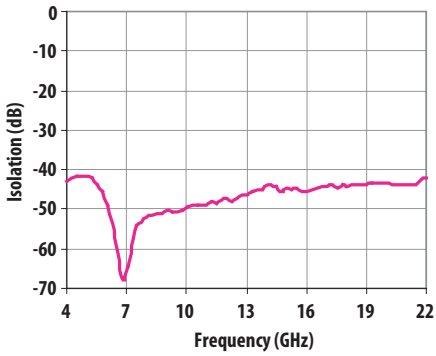


Figure 2. Isolation

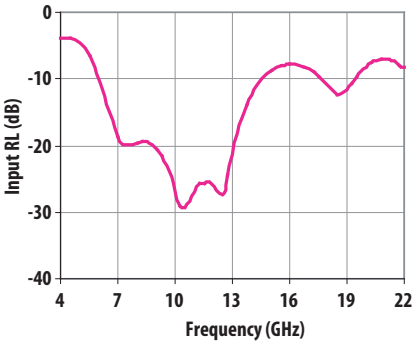


Figure 3. Input Return Loss

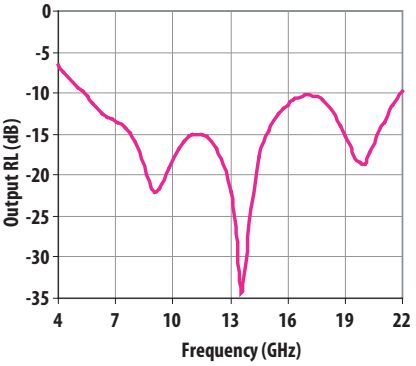


Figure 4. Output Return Loss

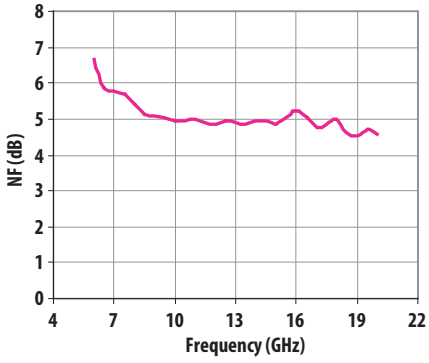


Figure 5. Noise Figure

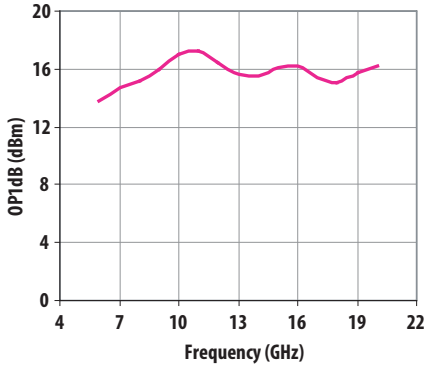


Figure 6. P1dB

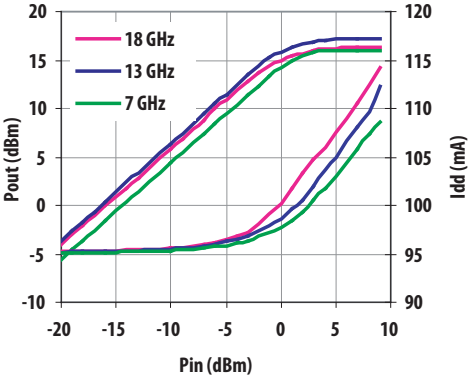


Figure 7. Pout and Idd vs. Pin

Note: These measurements are obtained using demo board with 50 Ohm traces at input and output. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity or low noise matching.

Over Voltage plots

All data measured on at Vdd = 5V, Idd = 95mA, Ta = 25oC, and 50 Ω at all ports.

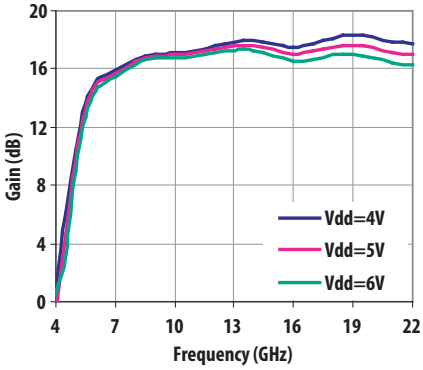


Figure 8. Gain and Voltage

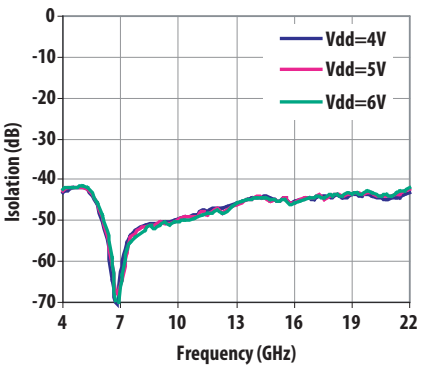


Figure 9. Isolation and Voltage

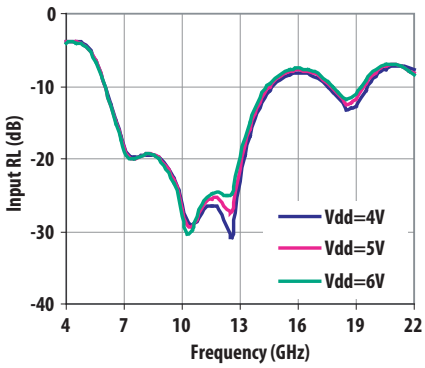


Figure 10. Input Return Loss and Voltage

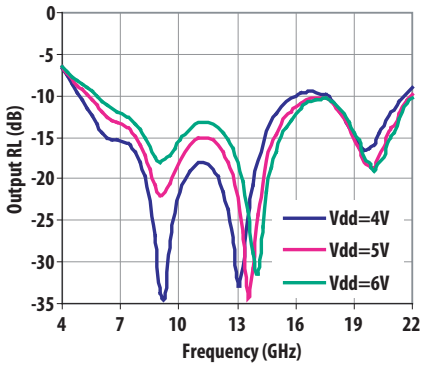


Figure 11. Output Return Loss and Voltage

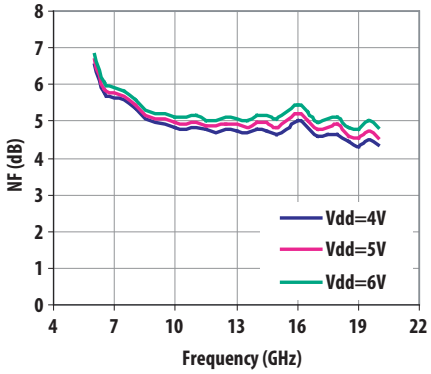


Figure 12. Noise Figure and Voltage

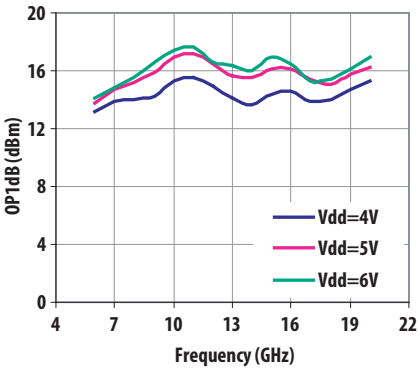


Figure 13. P1dB and Voltage

Note: These measurements are obtained using demo board with 50 Ohm traces at input and output. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity or low noise matching.

Over Temperature Performance Plots

All data measured on at Vdd = 5V, Idd = 95mA, Ta = 25oC, and 50 Ω at all ports

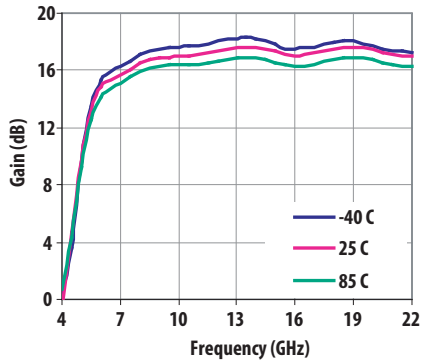


Figure 14. Gain and Temperature

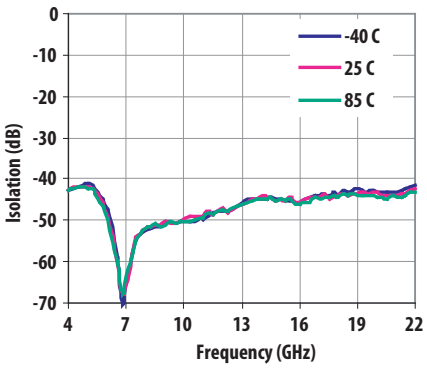


Figure 15. Isolation and Temperature

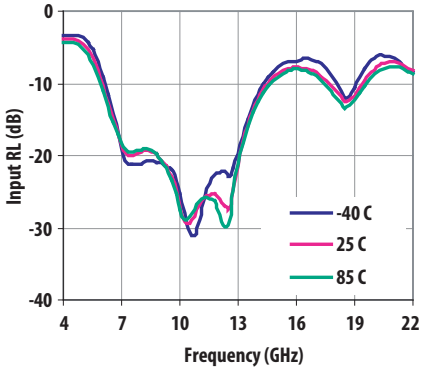


Figure 16. Input Return Loss and Temperature

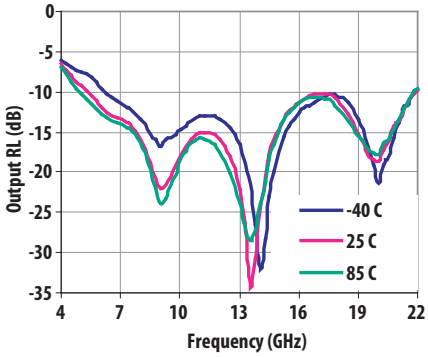


Figure 17. Output Return Loss and Temperature

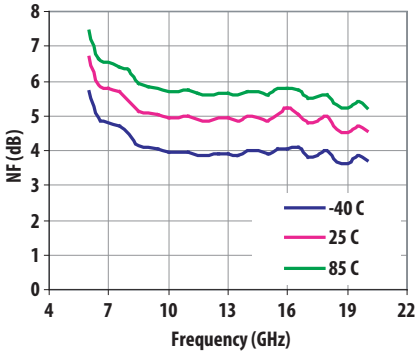


Figure 18. Noise Figure and Temperature

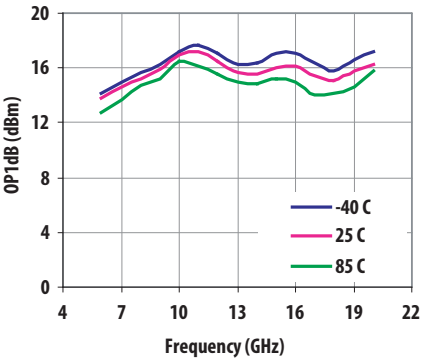


Figure 19. P1dB and Temperature

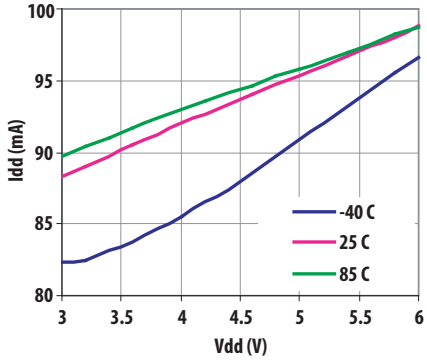


Figure 20. Idd vs. Vdd

Note: These measurements are obtained using demo board with 50 Ohm traces at input and output. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity or low noise matching.

Biasing and Operation

The AMMP-5620 only requires a single positive supply connected to the Vd pin (2). The recommended supply voltage is 5V. The supply should be bypassed with a 0.1uF capacitor placed as close to the component as possible. The package base is the RF and DC ground connection. The biasing arrangement is shown in Figure 21.

Figure 22 shows a simplifies schematic for the amplifier die. All three stages are self-biased as shown. Each stage has feedback around it to control the gain, match and performance, resulting in excellent wideband performance. Also shown are the on-chip DC blocking capacitors for both the RFin and RFout pins.

Please refer to the Absolute Maximum Ratings table for allowed DC and thermal conditions.

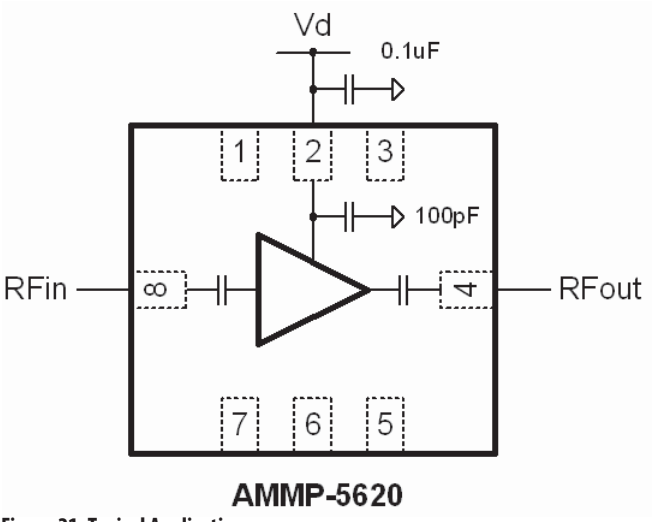


Figure 21. Typical Application

The AMMP Packaged Devices are compatible with high volume surface mount PCB assembly processes.

The PCB material and mounting pattern, as defined in the data sheet, optimizes RF performance and is strongly recommended. An electronic drawing of the land pattern is available upon request from Avago Sales & Application Engineering.

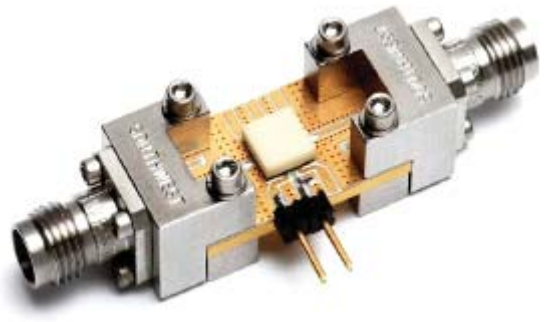


Figure 23. Demonstration Board (available upon request)

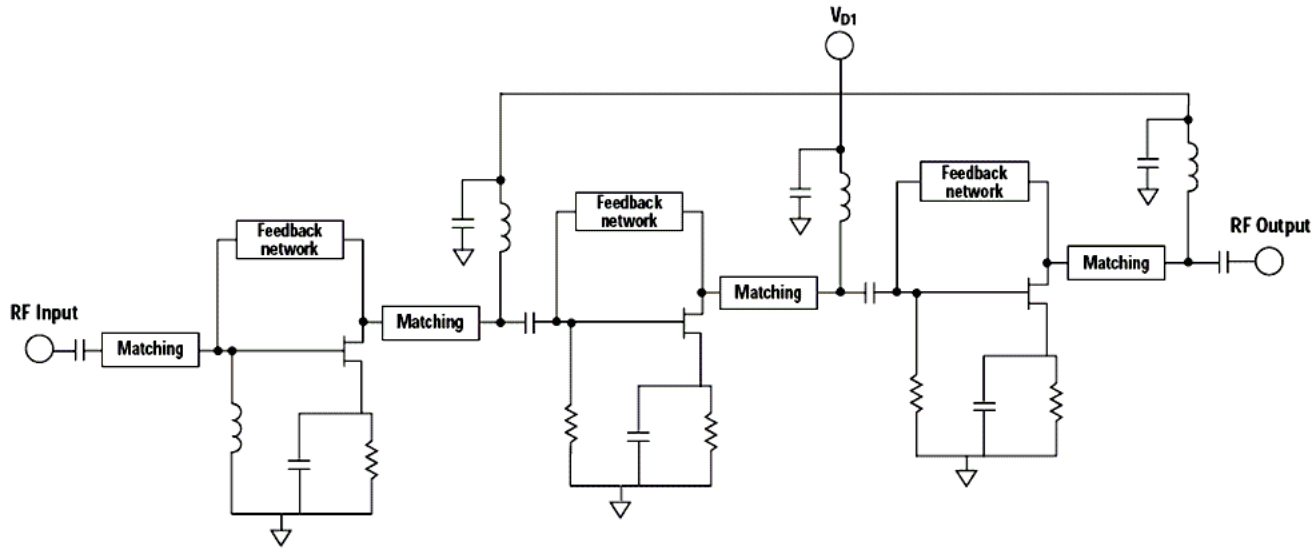


Figure 22. Simplified MMIC Schematics

Typical Scattering Parameters

Please refer to <http://www.avagotech.com> for typical scattering parameters data.

Package Dimension, PCB Layout and Tape and Reel information

Please refer to Avago Technologies Application Note 5520, AMxP-xxxx production Assembly Process (Land Pattern A).

Part Number Ordering Information

Part Number	Devices per Container	Container
AMMP-5620-BLKG	10	Antistatic Bag
AMMP-5620-TR1G	100	7" Reel
AMMP-5620-TR2G	500	7" Reel

Names and Contents of the Toxic and Hazardous Substances or Elements in the Products
产品中有毒有害物质或元素的名称及含量

Part Name 部件名称	Toxic and Hazardous Substances or Elements 有毒有害物质或元素					
	Lead (Pb) 铅 (Pb)	Mercury (Hg) 汞 （Hg ）	Cadmium (Cd) 镉 （Cd ）	Hexavalent (Cr(VI)) 六价铬（Cr(VI) ）	Polybrominated biphenyl (PBB) 多溴联苯（PBB ）	Polybrominated diphenylether (PBDE) 多溴二苯醚（PBDE ）
100pF capacitor	×	O	O	O	O	O

O: indicates that the content of the toxic and hazardous substance in all the homogeneous materials of the part is below the concentration limit requirement as described in SJ/T 11363-2006.
×: indicates that the content of the toxic and hazardous substance in at least one homogeneous material of the part exceeds the concentration limit requirement as described in SJ/T 11363-2006.
(The enterprise may further explain the technical reasons for the "x" indicated portion in the table in accordance with the actual situations.)

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。
×：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。
（企业可在此处，根据实际情况对上表中打"×" 的技术原因进行进一步说明。）

Note: EU RoHS compliant under exemption clause of "lead in electronic ceramic parts (e.g. piezoelectronic devices)"

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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