59C11

1K 5.0V CMOS Serial EEPROM

FEATURES

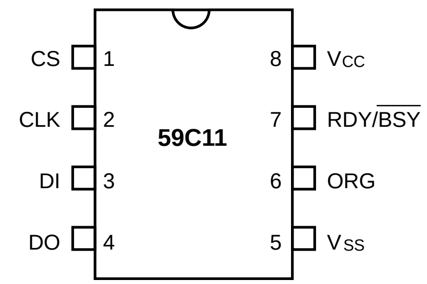
- Low power CMOS technology
- Pin selectable memory organization
  - 128 x 8 or 64 x 16 bit organization
- Single 5 volt only operation
- Self timed WRITE, ERAL and WRAL cycles
- Automatic erase before WRITE
- RDY/$\overline{\text{BSY}}$ status information during WRITE
- Power on/off data protection circuitry
- **1,000,000 ERASE/WRITE cycles guaranteed**
- Data Retention > 200 Years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - Commercial: 0˚C to +70˚C
  - Industrial: -40˚C to +85˚C
  - Automotive: -40˚C to +125˚C

DESCRIPTION

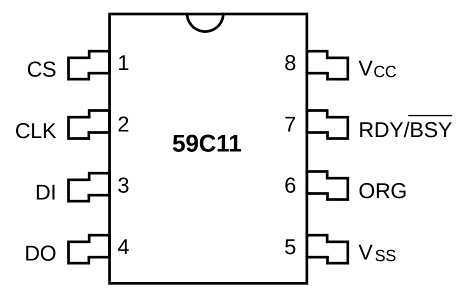
The Microchip Technology Inc. 59C11 is a 1K bit Electrically Erasable PROM. The device is configured as 128 x 8 or 64 x 16, selectable externally by means of the control pin ORG. Advanced CMOS technology makes this device ideal for low power nonvolatile memory applications. The 59C11 is available in the standard 8-pin DIP and a surface mount SOIC package.

PACKAGE TYPE

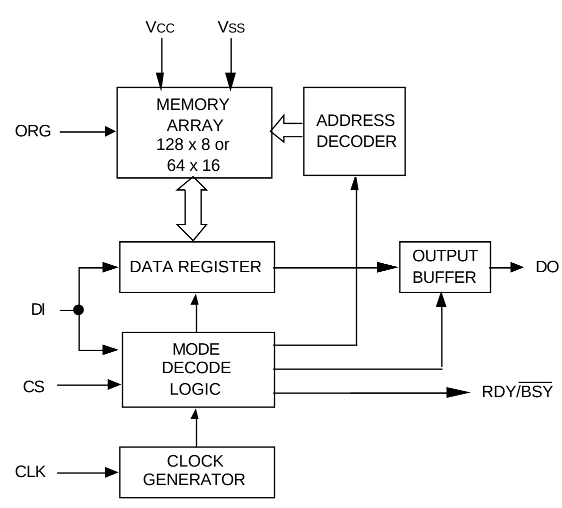
DIP



SOIC



BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC}.. 7.0V

All inputs and outputs w.r.t. V_{SS} ..... -0.6V to V_{CC} +1.0V

Storage temperature ....-65˚C to +150˚C

Ambient temperature with
power applied.....................................-65˚C to +125˚C

Soldering temperature of leads (10 seconds) ...+300˚C

ESD protection on all pins.................................... 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
V_{SS}	Ground
ORG	Memory Array Organization
RDY/$\overline{\text{BSY}}$	Ready/$\overline{\text{Busy}}$ Status
V_{CC}	+5V Power SUpply

TABLE 1-2: DC CHARACTERISTICS

V_{CC} = +5V (±10%)

Commercial: Tamb = 0°C to 70°C
Industrial: Tamb = -40°C to +85°C
Automotive: Tamb = -40°C to 125°C

Parameter	Symbol	Min	Max	Units	Conditions
V_{CC} detector threshold	V_{TH}	2.8	4.5	V	
High level input voltage	V_{IH}	2.0	Vcc+1	V	
Low level input voltage	V_{IL}	-0.3	0.8	V	
High level output voltage	V_{OH}	2.4	—	V	I_{OH} = -400 µA
Low level output voltage	V_{OL}	—	0.4	V	I_{OL} = 3.2 mA
Input leakage current	I_{LI}	—	10	µA	V_{IN} = 0V to V_{CC} (Note 1)
Output leakage current	I_{LO}	—	10	µA	V_{OUT} = 0V to V_{CC} (Note 1)
Pin capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	7	pF	V_{IN}/V_{OUT} = 0V (Note 2) Tamb = 25°C, f = 1 MHz
Operating current (all modes)	I_{CC} write	—	4	mA	F_{CLK} = 1 MHz, V_{CC} = 5.5V
Standby current	I_{CCS}	—	100	µA	CS = 0V, V_{CC} = 5.5V

Note 1: Internal resister pull-up at Pin 6. Active output at Pin 7.
Note 2: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: SYNCHRONOUS DATA TIMING

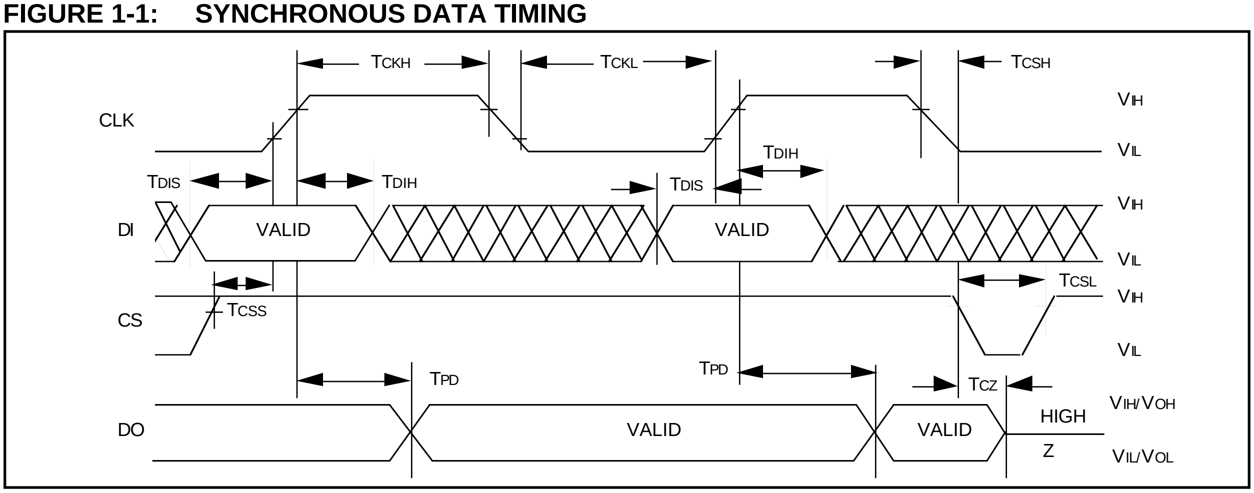


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	F_{CLK}		1	MHz	
Clock high time	T_{CKH}	500	—	ns	
Clock low time	T_{CKL}	500	—	ns	
Chip select setup time	T_{CSS}	50	—	ns	
Chip select hold time	T_{CSH}	0	—	ns	
Chip select low time	T_{CS}	100	—	ns	
Data input setup time	T_{DIS}	100	—	ns	
Data input hold time	T_{DIH}	100	—	ns	
Data output delay time	T_{PD}	—	400	ns	CL = 100 pF
Data output disable time (from CS = low)	T_{CZ}	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	T_{DDZ}	0	400	ns	CL = 100 pF
RDY/$\overline{\text{BSY}}$ delay time	T_{RBD}	—	400	ns	
Program cycle time (Auto Erase and Write)	Twc	—	1 15	ms ms	for 8-bit mode for ERAL and WRAL in 8/16-bit modes

2.0 PIN DESCRIPTION

2.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a WRITE cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a WRITE cycle, the device will go into standby mode as soon as the WRITE cycle is completed.

CS must be LOW for 100 ns (T_{CSL}) minimum between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

2.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 59C11. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock high time (T_{CKH}) and clock low time (T_{CKL})). This gives freedom in preparing opcode, address and data for the controlling master.

CLK is a “Don't Care” if CS is LOW (device deselected). If CS is HIGH, but a START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto erase/write) cycle.

After detection of a START condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). When that limit has been reached, CLK and DI become “Don't Care” inputs until CS is brought LOW for at least chip select low time (T_{CSL}) and brought HIGH again and a WRITE cycle (if any) is completed.

2.3 Data In (DI)

Data In is used to clock in START bit, opcode, address and data synchronously with the CLK input.

2.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (T_{PD} after the positive edge of CLK). This output is in HIGH–Z mode except if data is clocked out as a result of a READ instruction.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is output after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during WRITE cycles.

2.5 Organization (ORG)

This input selects the memory array organization. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 64 x 16 organization. In applications subject to electrical noise, it is recommended that this pin not be left floating, but tied either high or low.

2.6 Ready/Busy (RDY/$\overline{BSY}$)

Pin 7 provides RDY/$\overline{BSY}$ status information. RDY/BSY is low if the device is performing a WRITE, ERAL, or WRAL operation. When it is HIGH the internal, self-timed WRITE, ERAL or WRAL operation has been completed and the device is ready to receive a new instruction.

3.0 DATA PROTECTION

During power-up, all modes of operation are inhibited until VCC has reached a level of 2.8 V. During power-down, the source data protection circuitry acts to inhibit all modes when VCC has fallen below 2.8 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, EWEN instruction must be performed before any WRITE, ERAL or WRAL instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

TABLE 3-1: INSTRUCTION SET

6 X 16 MODE, ORG = 1						
Instruction	**Start Bit**	**Opcode**	**Address**	**Data In**	**Data Out**	**Number of Req. CLK CYcles**
READ	1	1 0 X X	A5 A4 A3 A2 A1 A0	—	D15-D0	27
WRITE	1	X 1 X X	A5 A4 A3 A2 A1 A0	D15-D0	High-Z	27
EWEN	1	0 0 1 1	X X X X X X	—	High-Z	11
EWDS	1	0 0 0 0	X X X X X X	—	High-Z	11
ERAL	1	0 0 1 0	X X X X X X	—	High-Z	11
WRAL	1	0 0 0 1	X X X X X X	D15-D0	High-Z	27
128 X 8 MODE, ORG = 0						
Instruction	**Start Bit**	**Opcode**	**Address**	**Data In**	**Data Out**	**Number of Req. CLK CYcles**
READ	1	1 0 X X	A6 A5 A4 A3 A2 A1 A0	—	D7-D0	20
WRITE	1	X 1 X X	A6 A5 A4 A3 A2 A1 A0	D7-D0	High-Z	20
EWEN	1	0 0 1 1	X X X X X X X	—	High-Z	12
EWDS	1	0 0 0 0	X X X X X X X	—	High-Z	12
ERAL	1	0 0 1 0	X X X X X X X	—	High-Z	12
WRAL	1	0 0 0 1	X X X X X X X	D7-D0	High-Z	20

4.0 FUNCTIONAL DESCRIPTION

4.1 START Condition

The START bit is detected by the device if CS and DI are both High with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition) without resulting in any device operation (READ, WRITE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e. clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

Note:	CS must go LOW between consecutive instructions.

4.2 DI/DO Pins

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a “bus conflict” to occur during the “dummy zero” that precedes the READ operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

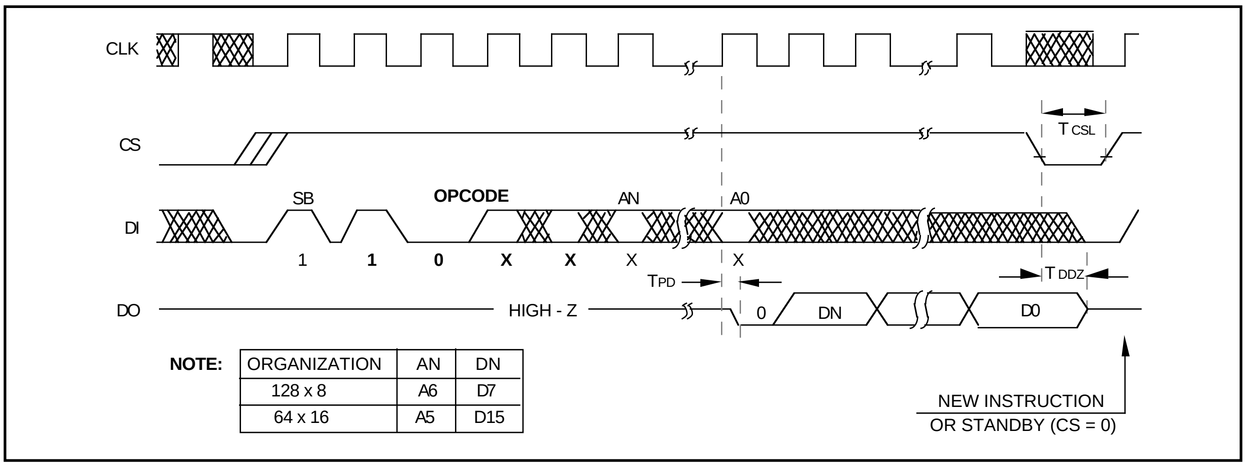
4.3 READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 8- or 16-bit output string. The output data changes during the high state of the system clock (CLK). The dummy bit is output T_{PD} after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 is a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the negative edge of CS, whichever occurs first. D0 remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

The most significant data bit (D15 or D7) is always output first, followed by the lower significant bits (D14 - D0 or D6 - D0).

FIGURE 4-1: READ MODE

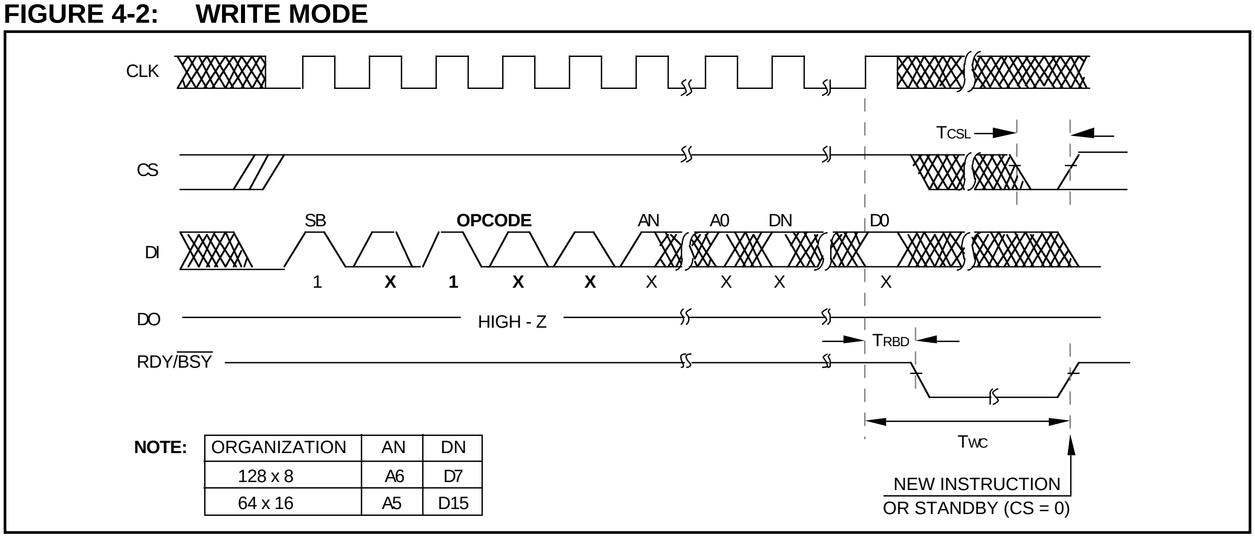


4.4 WRITE

The WRITE instruction is followed by 8 or 16 bits of data which are written into the specified address. The most significant data bit (D15 or D7) has to be clocked in first followed by the lower significant data bits (D14 – D0 or D6 – D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic erase cycle on the specified address before the data are written. The WRITE cycle is completely self timed and commences automatically after the rising edge of the CLK signal for the last data bit (D0).

The WRITE cycle takes 1 ms maximum for 8-bit mode and 2 ms maximum for 16-bit mode.

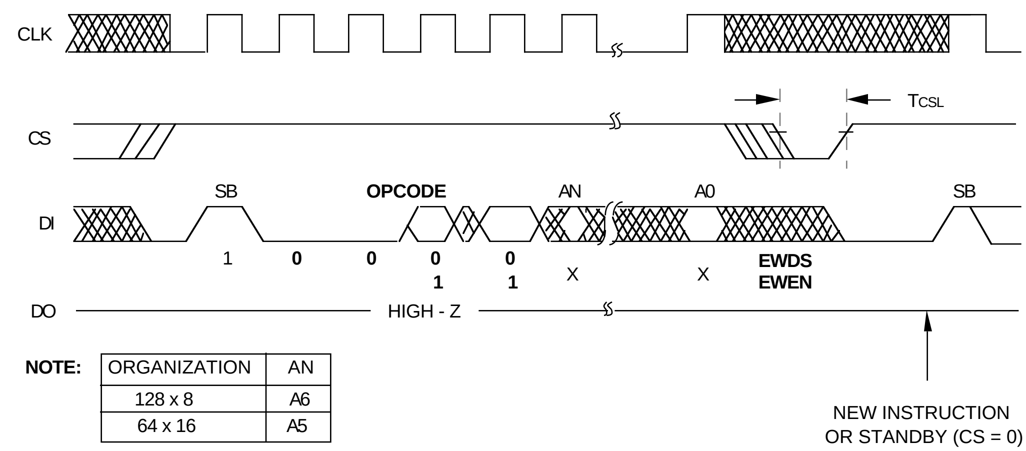
FIGURE 4-2: WRITE MODE



4.5 ERASE/WRITE Enable/Disable (EWEN, EWDS)

The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, EWEN instruction has to be performed before any WRITE, ERAL, or WRAL instruction is executed by the device. For added data protection, the device should be put in the ERASE/WRITE Disable mode (EWDS) after programming operations are completed.

FIGURE 4-3: ERASE/WRITE ENABLE AND DISABLE



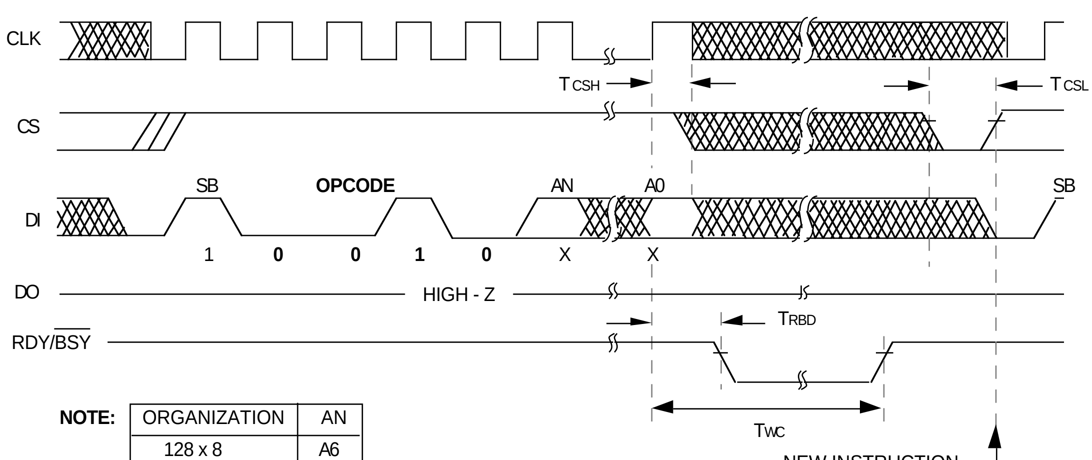
NOTE:

ORGANIZATION	AN
128 x 8	A6
64 x 16	A5

4.6 ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the rising edge of the CLK signal for the last dummy address bit. ERAL takes 15 ms maximum.

FIGURE 4-4: ERASE ALL (ERAL)



NOTE:

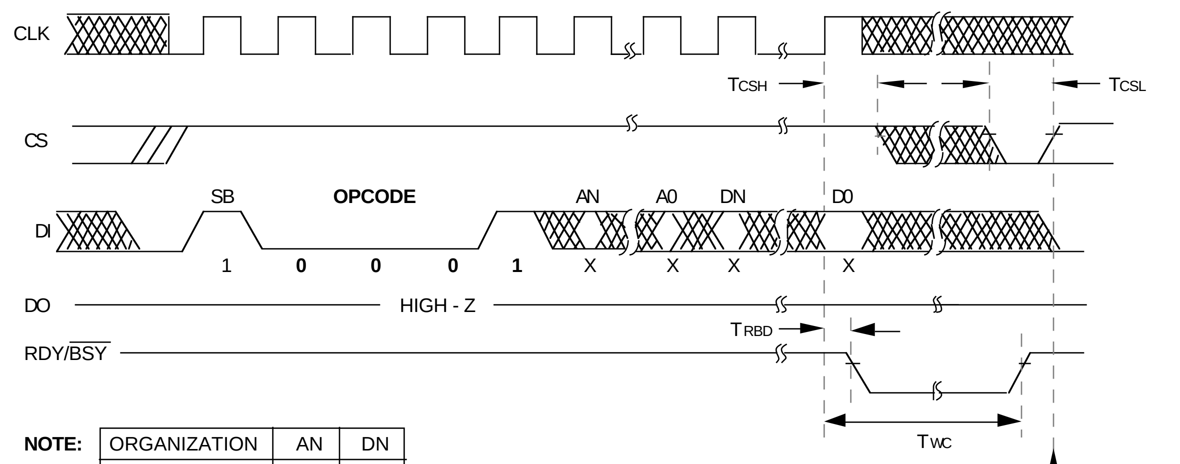
ORGANIZATION	AN
128 x 8	A6
64 x 16	A5

4.7 WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the last data bit (D0) has been clocked in. WRAL takes 15 ms maximum.

Note:	The WRAL does not include an automatic ERASE cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases. The WRAL instruction is used for testing and/or device initialization.

FIGURE 4-5: WRITE ALL



NOTE:

ORGANIZATION	AN	DN
128 x 8	A6	D7
64 x 16	A5	D15

59C11 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

59C11 - I /P

Package:	P =	Plastic DIP (300 mil Body)
	SN =	Plastic SOIC (150 mil Body)
	SM =	Plastic SOIC (207 mil Body)
Temperature Range:	Blank =	0°C to +70°C
	I =	-40°C to +85°C
	E =	-40°C to +125°C
Device:	59C11	1K CMOS Serial EEPROM
	59C11T	1K CMOS Serial EEPROM (Tape and Reel)

AMERICAS

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