

## 128K (16K x 8) CMOS EPROM

### FEATURES

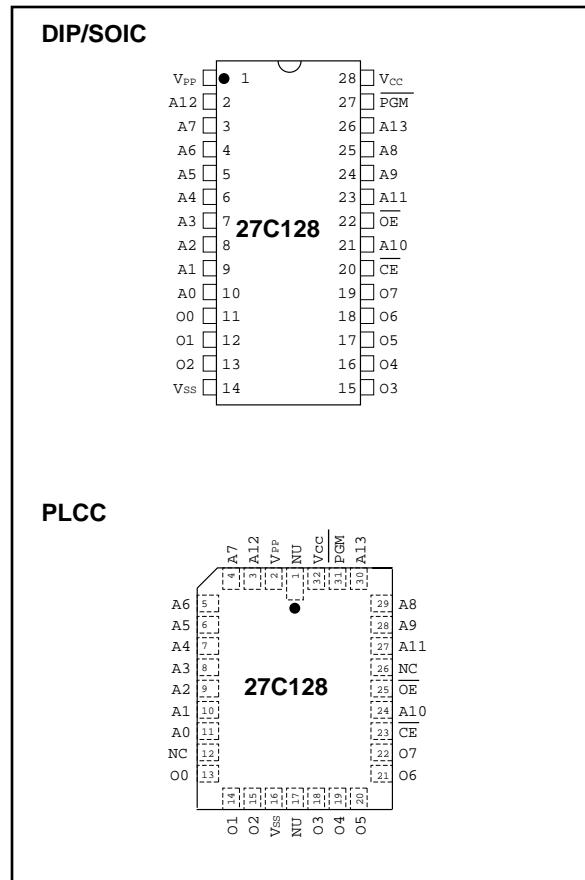
- High speed performance
  - 120 ns access time available
- CMOS Technology for low power consumption
  - 20 mA Active current
  - 100  $\mu$ A Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 16K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC Package
  - 28-pin SOIC package
  - Tape and reel
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

### DESCRIPTION

The Microchip Technology Inc. 27C128 is a CMOS 128K bit (electrically) Programmable Read Only Memory. The device is organized as 16K words by 8 bits (16K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120 ns. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements. A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC, or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages. UV erasable versions are also available.

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### PACKAGE TYPE



## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Maximum Ratings\*

VCC and input voltages w.r.t. VSS..... -0.6V to +7.25V  
 VPP voltage w.r.t. VSS during programming..... -0.6V to +14V  
 Voltage on A9 w.r.t. VSS ..... -0.6V to +13.5V  
 Output voltage w.r.t. VSS .....-0.6V to VCC +1.0V  
 Storage temperature .....-65°C to +150°C  
 Ambient temp. with power applied .....-65°C to +125°C

\*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = +5V (±10%) Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C Extended (Automotive): Tamb = -40°C to +125°C							
Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	V <sub>IH</sub> V <sub>IL</sub>	2.0 -0.5	V <sub>CC</sub> +1 0.8	V V	
Input Leakage	all	—	I <sub>LI</sub>	-10	10	µA	V <sub>IN</sub> = 0 to V <sub>CC</sub>
Output Voltages	all	Logic "1" Logic "0"	V <sub>OH</sub> V <sub>OL</sub>	2.4	0.45	V V	I <sub>OH</sub> = -400 µA I <sub>OL</sub> = 2.1 mA
Output Leakage	all	—	I <sub>LO</sub>	-10	10	µA	V <sub>OUT</sub> = 0V to V <sub>CC</sub>
Input Capacitance	all	—	C <sub>IN</sub>	—	6	pF	V <sub>IN</sub> = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	C <sub>OUT</sub>	—	12	pF	V <sub>OUT</sub> = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I,E	TTL input TTL input	I <sub>CC1</sub> I <sub>CC2</sub>	— —	20 25	mA mA	V <sub>CC</sub> = 5.5V; V <sub>PP</sub> = V <sub>CC</sub> f = 1 MHz; $\overline{OE} = \overline{CE} = V_{IL}$ ; I <sub>OUT</sub> = 0 mA; V <sub>IL</sub> = -0.1 to 0.8V; V <sub>IH</sub> = 2.0 to V <sub>CC</sub> ; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	I <sub>CC(s)</sub>	— — —	2 3 100	mA mA µA	$\overline{CE} = V_{CC} \pm 0.2V$
I <sub>PP</sub> Read Current V <sub>PP</sub> Read Voltage	all all	Read Mode Read Mode	I <sub>PP</sub> V <sub>PP</sub>	V <sub>CC</sub> -0.7	100 V <sub>CC</sub>	µA V	V <sub>PP</sub> = 5.5V Note 2

\* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

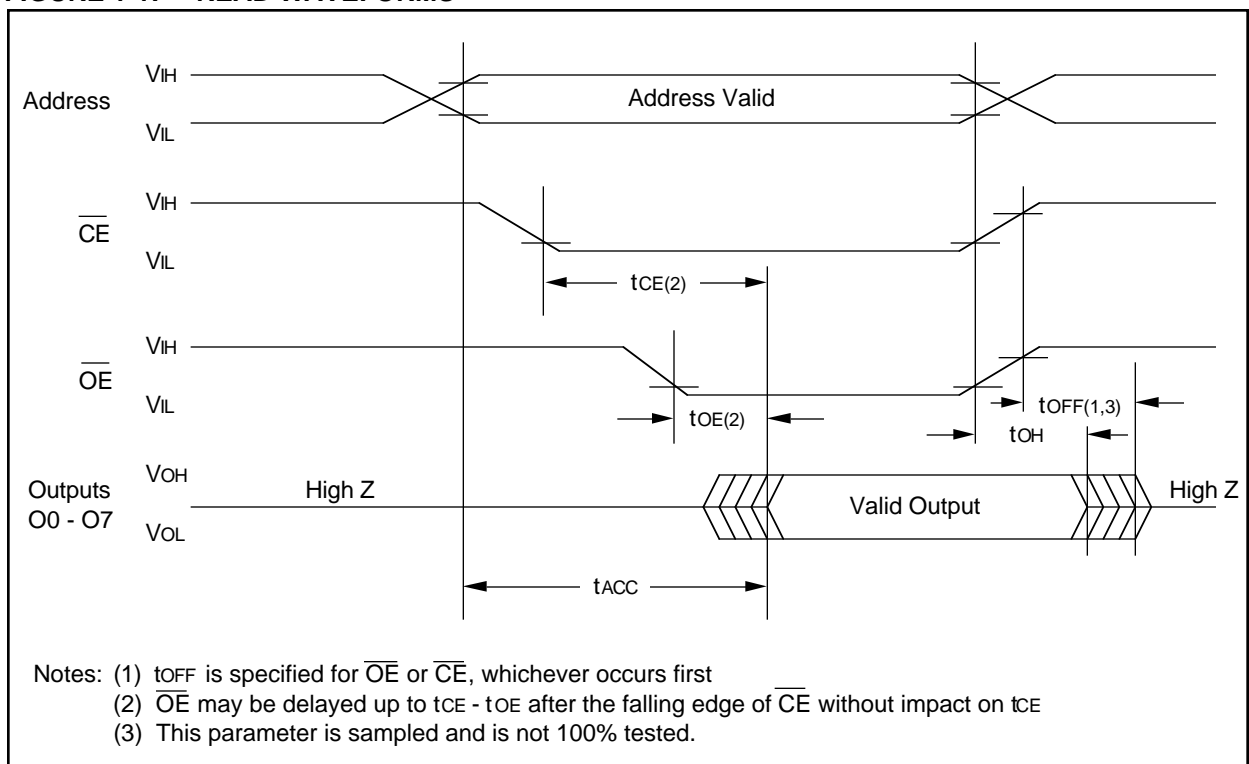
Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

Note 2: V<sub>CC</sub> must be applied before V<sub>PP</sub>, and be removed simultaneously or after V<sub>PP</sub>.

**TABLE 1-3: READ OPERATION AC CHARACTERISTICS**

Parameter	Sym	AC Testing Waveform: $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$ ; $V_{OH} = 2.0V$ $V_{OL} = 0.8V$ Output Load: 1 TTL Load + 100 pF Input Rise and Fall Times: 10 ns Ambient Temperature: Commercial: $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ Industrial: $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$ Extended (Automotive): $T_{amb} = -40^{\circ}C$ to $+125^{\circ}C$										Units	Conditions
		27C128-12		27C128-15		27C128-17		27C128-20		27C128-25			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	$t_{ACC}$	—	120	—	150	—	170	—	200	—	250	ns	$\overline{CE}=\overline{OE}=V_{IL}$
$\overline{CE}$ to Output Delay	$t_{CE}$	—	120	—	150	—	170	—	200	—	250	ns	$\overline{OE}=V_{IL}$
$\overline{OE}$ to Output Delay	$t_{OE}$	—	65	—	70	—	70	—	75	—	100	ns	$\overline{CE}=V_{IL}$
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	$t_{OFF}$	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$ , whichever occurs first	$t_{OH}$	0	—	0	—	0	—	0	—	0	—	ns	

**FIGURE 1-1: READ WAVEFORMS**



**TABLE 1-4: PROGRAMMING DC CHARACTERISTICS**

Ambient Temperature: $T_{amb} = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ $V_{CC} = 6.5\text{V} \pm 0.25\text{V}$ , $V_{PP} = 13.0\text{V} \pm 0.25\text{V}$						
Parameter	Status	Symbol	Min	Max.	Units	Conditions
Input Voltages	Logic"1"	$V_{IH}$	2.0	$V_{CC}+1$	V	
	Logic"0"	$V_{IL}$	-0.1	0.8	V	
Input Leakage	—	$I_{LI}$	-10	10	$\mu\text{A}$	$V_{IN} = 0\text{V to } V_{CC}$
Output Voltages	Logic"1"	$V_{OH}$	2.4		V	$I_{OH} = -400 \mu\text{A}$
	Logic"0"	$V_{OL}$		0.45	V	$I_{OL} = 2.1 \text{ mA}$
VCC Current, program & verify	—	$I_{CC2}$	—	20	mA	Note 1
VPP Current, program	—	$I_{PP2}$	—	25	mA	Note 1
A9 Product Identification	—	$V_H$	11.5	12.5	V	

Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP

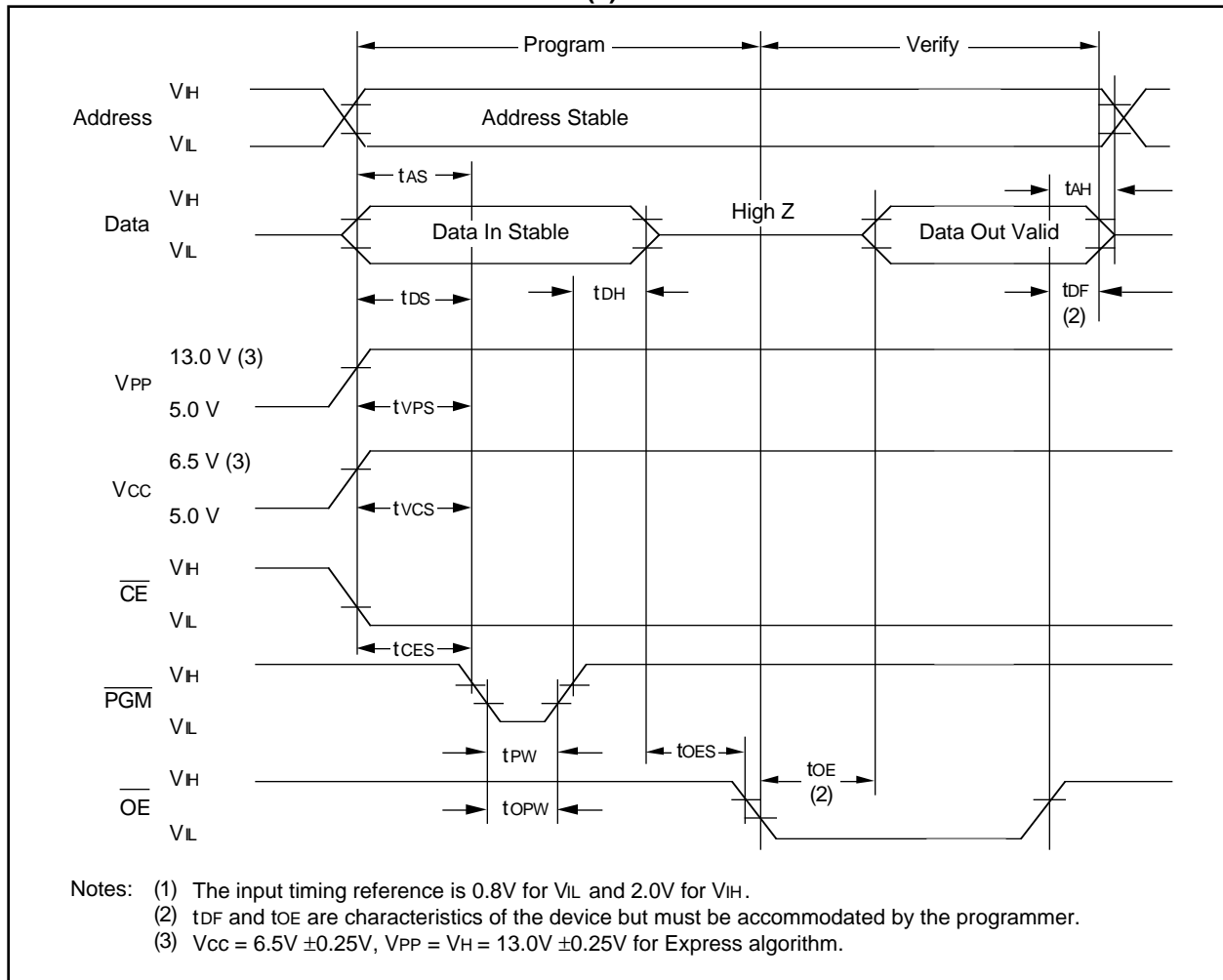
**TABLE 1-5: PROGRAMMING AC CHARACTERISTICS**

for Program, Program Verify and Program Inhibit Modes		AC Testing Waveform: $V_{IH}=2.4\text{V}$ and $V_{IL}=0.45\text{V}$ ; $V_{OH}=2.0\text{V}$ ; $V_{OL}=0.8\text{V}$ Ambient Temperature: $T_{amb}=25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ $V_{CC}= 6.5\text{V} \pm 0.25\text{V}$ , $V_{PP} = V_H = 13.0\text{V} \pm 0.25\text{V}$				
Parameter	Symbol	Min	Max	Units	Remarks	
Address Set-Up Time	tAS	2	—	$\mu\text{s}$		
Data Set-Up Time	tDS	2	—	$\mu\text{s}$		
Data Hold Time	tDH	2	—	$\mu\text{s}$		
Address Hold Time	tAH	0	—	$\mu\text{s}$		
Float Delay (2)	tDF	0	130	ns		
VCC Set-Up Time	tVCS	2	—	$\mu\text{s}$		
Program Pulse Width (1)	tPW	95	105	$\mu\text{s}$	100 $\mu\text{s}$ typical	
$\overline{\text{CE}}$ Set-Up Time	tCES	2	—	$\mu\text{s}$		
$\overline{\text{OE}}$ Set-Up Time	tOES	2	—	$\mu\text{s}$		
VPP Set-Up Time	tVPS	2	—	$\mu\text{s}$		
Data Valid from $\overline{\text{OE}}$	tOE	—	100	ns		

Note 1: For express algorithm, initial programming width tolerance is  $100 \mu\text{s} \pm 5\%$ .

Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

**FIGURE 1-2: PROGRAMMING WAVEFORMS (1)**



**TABLE 1-6: MODES**

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V <sub>PP</sub>	A <sub>9</sub>	O <sub>0</sub> - O <sub>7</sub>
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>CC</sub>	X	DOUT
Program	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>H</sub>	X	DIN
Program Verify	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>H</sub>	X	DOUT
Program Inhibit	V <sub>IH</sub>	X	X	V <sub>H</sub>	X	High Z
Standby	V <sub>IH</sub>	X	X	V <sub>CC</sub>	X	High Z
Output Disable	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>CC</sub>	X	High Z
Identity	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>CC</sub>	V <sub>H</sub>	Identity Code

X = Don't Care

## 1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

- the  $\overline{CE}$  pin is low to power up (enable) the chip
- the  $\overline{OE}$  pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (t<sub>ACC</sub>) is equal to the delay from  $\overline{CE}$  to output (t<sub>CE</sub>). Data is transferred to the output after a delay from the falling edge of  $\overline{OE}$  (t<sub>OE</sub>).

## 1.3 Standby Mode

The standby mode is defined when the  $\overline{CE}$  pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100  $\mu$ A.

## 1.4 Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The  $\overline{OE}$  and  $\overline{PGM}$  pins are both high.

## 1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm<sup>2</sup> is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 $\mu$ W/cm<sup>2</sup> for approximately 20 minutes.

## 1.6 Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

- VCC is brought to the proper voltage,
- VPP is brought to the proper VH level,
- the  $\overline{CE}$  pin is low,
- the  $\overline{OE}$  pin is high, and
- the  $\overline{PGM}$  pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A13 and the data to be programmed is presented to pins O0-O7. When data and address are stable,  $\overline{OE}$  is high,  $\overline{CE}$  is low and a low-going pulse on the  $\overline{PGM}$  line programs that location.

## 1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

- VCC is at the proper level,
- VPP is at the proper VH level,
- the  $\overline{CE}$  line is low,
- the  $\overline{PGM}$  line is high, and
- the  $\overline{OE}$  line is low.

## 1.8 Inhibit

When programming multiple devices in parallel with different data, only  $\overline{CE}$  or  $\overline{PGM}$  need be under separate control to each device. By pulsing the  $\overline{CE}$  or  $\overline{PGM}$  line low on a particular device in conjunction with the  $\overline{PGM}$  or  $\overline{CE}$  line low, that device will be programmed; all other devices with  $\overline{CE}$  or  $\overline{PGM}$  held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on  $\overline{CE}$  or  $\overline{PGM}$ ); and the device is inhibited from programming.

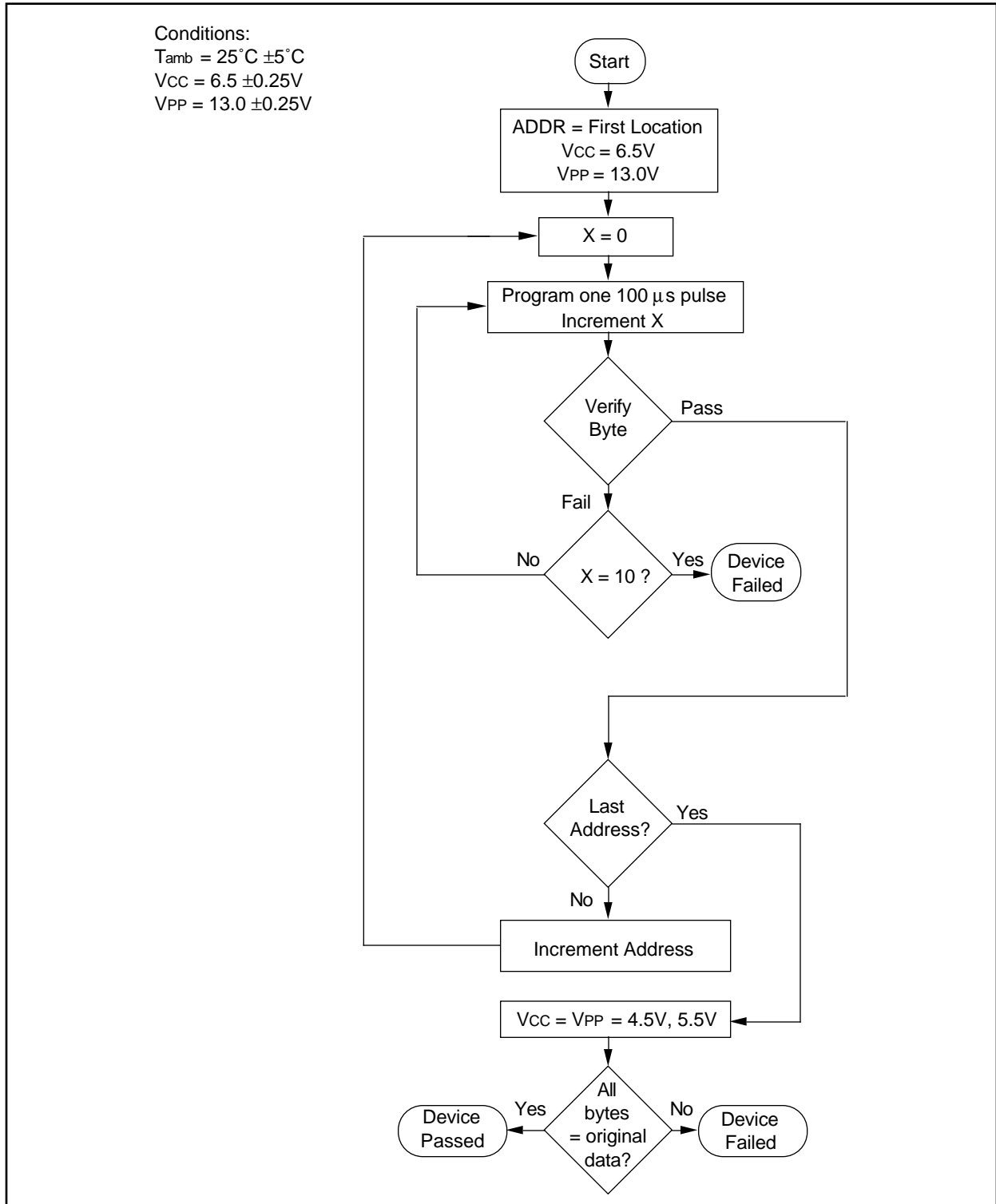
## 1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The  $\overline{CE}$  and  $\overline{OE}$  lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin $\rightarrow$	Input	Output								
Identity $\downarrow$	A0	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	H e x
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	0	0	1	1	83

\* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



# 27C128

## 27C128 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

<b>27C128 - 25</b>	<b>I</b>	<b>/P</b>		
			<b>Package:</b>	L Plastic Leaded Chip Carrier (PLCC) P Plastic DIP SO Plastic SOIC
			<b>Temperature Range:</b>	- 0°C to +70°C I -40°C to +85°C E -40°C to +125°C
			<b>Access Time:</b>	12 120 ns 15 150 ns 17 170 ns 20 200 ns 25 250 ns
			<b>Device:</b>	27C128 128K (16K x 8) CMOS EPROM

### AMERICAS

#### Corporate Office

Microchip Technology Inc.  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 602 786-7200 Fax: 602 786-7277  
Technical Support: 602 786-7627  
Web: <http://www.mchip.com/biz/mchip>

#### Atlanta

Microchip Technology Inc.  
500 Sugar Mill Road, Suite 200B  
Atlanta, GA 30350  
Tel: 770 640-0034 Fax: 770 640-0307

#### Boston

Microchip Technology Inc.  
5 Mount Royal Avenue  
Marlborough, MA 01752  
Tel: 508 480-9990 Fax: 508 480-8575

#### Chicago

Microchip Technology Inc.  
333 Pierce Road, Suite 180  
Itasca, IL 60143  
Tel: 708 285-0071 Fax: 708 285-0075

#### Dallas

Microchip Technology Inc.  
14651 Dallas Parkway, Suite 816  
Dallas, TX 75240-8809  
Tel: 214 991-7177 Fax: 214 991-8588

#### Dayton

Microchip Technology Inc.  
35 Rockridge Road  
Englewood, OH 45322  
Tel: 513 832-2543 Fax: 513 832-2841

#### Los Angeles

Microchip Technology Inc.  
18201 Von Karman, Suite 455  
Irvine, CA 92715  
Tel: 714 263-1888 Fax: 714 263-1338

#### New York

Microchip Technology Inc.  
150 Motor Parkway, Suite 416  
Hauppauge, NY 11788  
Tel: 516 273-5305 Fax: 516 273-5335

### AMERICAS (continued)

#### San Jose

Microchip Technology Inc.  
2107 North First Street, Suite 590  
San Jose, CA 95131  
Tel: 408 436-7950 Fax: 408 436-7955

### ASIA/PACIFIC

#### Hong Kong

Microchip Technology  
Unit No. 3002-3004, Tower 1  
Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T. Hong Kong  
Tel: 852 2 401 1200 Fax: 852 2 401 3431

#### Korea

Microchip Technology  
168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku,  
Seoul, Korea  
Tel: 82 2 554 7200 Fax: 82 2 558 5934

#### Singapore

Microchip Technology  
200 Middle Road  
#10-03 Prime Centre  
Singapore 188980  
Tel: 65 334 8870 Fax: 65 334 8850

#### Taiwan

Microchip Technology  
10F-1C 207  
Tung Hua North Road  
Taipei, Taiwan, ROC  
Tel: 886 2 717 7175 Fax: 886 2 545 0139

### EUROPE

#### United Kingdom

Arizona Microchip Technology Ltd.  
Unit 6, The Courtyard  
Meadow Bank, Furlong Road  
Bourne End, Buckinghamshire SL8 5AJ  
Tel: 44 0 1628 851077 Fax: 44 0 1628 850259

#### France

Arizona Microchip Technology SARL  
2 Rue du Buisson aux Fraises  
91300 Massy - France  
Tel: 33 1 69 53 63 20 Fax: 33 1 69 30 90 79

#### Germany

Arizona Microchip Technology GmbH  
Gustav-Heinemann-Ring 125  
D-81739 Muenchen, Germany  
Tel: 49 89 627 144 0 Fax: 49 89 627 144 44

#### Italy

Arizona Microchip Technology SRL  
Centro Direzionale Colleoni  
Palazzo Pegaso Ingresso No. 2  
Via Paracelso 23, 20041  
Agrate Brianza (MI) Italy  
Tel: 39 039 689 9939 Fax: 39 039 689 9883

### JAPAN

Microchip Technology Intl. Inc.  
Benex S-1 6F  
3-18-20, Shin Yokohama  
Kohoku-Ku, Yokohama  
Kanagawa 222 Japan  
Tel: 81 45 471 6166 Fax: 81 45 471 6122

9/5/95



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Printed in the USA, 9/95  
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